

AMENDMENTS TO THE CLAIMS

Claims 1-17: (Canceled)

Claim 18 (Currently Amended): In a searcher, a method of determining a phase offset of a signal, the method comprising the steps of:

- a) receiving the signal having a first code sequence in a memory;
- b) receiving an additional signal having a second code sequence at a plurality of computation circuits;
- c) implementing a unique phase offset for the second code sequence in each of the plurality of computation circuits by temporarily storing the second code sequence in a memory buffer with varying size to provide the unique phase offset to each of the plurality of computation circuits; and
- d) multi-bit correlating the second code sequence having the unique phase offsets with the first code sequence in each of the respective plurality of computation circuits in a single clock cycle and in parallel.

Claims 19-25 (Canceled)

Claim 26 (Currently Amended): A communication device for processing data signals, the communication device comprising:

- a transceiver for receiving a signal having a first code sequence into a memory;

a code generator for generating a second code sequence;

a searcher coupled to the transceiver and to the code generator, the searcher having a plurality of computation circuits for multi-bit correlating in a single clock cycle and in parallel the first code sequence and the second code sequence at a plurality of offsets; and

at least one memory block coupled to at least one of the plurality of computation circuits, the memory block having a variable length to implement a variable offset between the first code sequence and the second code sequence.

Claims 27-28 (Canceled)

Claim 29 (New): The method of claim 18, wherein the memory buffer simultaneously receives and transmits to the computation circuits the second code sequence.

Claim 30 (New): The communication device of claim 26, wherein the memory block simultaneously receives and transmits to the computation circuits the second code sequence.

Claim 31 (New): The method of claim 18, wherein the memory for the first code sequence simultaneously receives the signal and transmits multiple signal samples in parallel to each of the plurality of computation circuits.

